DOCKET NO. STMI07-02021 **PATENT**
CUSTOMER NO. 23990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	Franck Badets et al.
Serial No.	:	10/603,579
Filed	:	June 25, 2003
For	:	VARIABLE PHASE-SHIFTING CIRCUIT, PHASE INTERPOLATOR INCORPORATING IT, AND DIGITAL FREQUENCY SYNTHESIZER INCORPORATING SUCH AN INTERPOLATOR
Group No.	:	2816
Examiner	:	Tuan Thieu Lam
Confirmation No.	:	4869

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Commissioner for Patents
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Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicants request review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal. The review is requested for the reasons stated in the arguments below, demonstrating the clear legal and factual deficiency of the rejections of some or all claims.

Claims 1, 2, 24-29 and 33-36 were finally rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,469,585 to Dai et al. ("*Dai*"). Claims 3, 30-32 and 37-39 contain allowable subject matter but were objected to as being dependent upon a rejected base claim.

Claims 4-23 have been previously withdrawn due to a restriction requirement.

The Examiner stated that the circuit shown in Figure 3 of the *Dai* reference anticipates the Applicants' invention as claimed in Claims 1-2, 24-29 and 33-36. (August 5, 2008 Office Action, Pages 2-3). The Applicants respectfully point out that the circuit that is shown in Figure 3 of the *Dai* reference is a delay stage 32 for a ring-type voltage controlled oscillator 30. The delay stage 32 comprises inverters (33 and 34), a memory circuit (35) and tuning circuitry (transistors M1, M4, M7 and M10). The transistors of the tuning circuitry function as variable resistors to tune the amount of delay of the delay stage 32, and hence the frequency of the voltage controlled oscillator 30. (*Dai*, Column 4, Lines 23-28). The frequency (not the phase) is tuned. Therefore, the *Dai* reference does not show a phase shifter circuit.

The *Dai* reference states that each delay stage (32A and 32B) causes a ninety degree phase shift. The *Dai* reference states "Each delay stage 32A and 32B causes a 90° phase shift, and so the phase shifts relative to V_{OUT+} of delay stage 32A are as follows – V_{OUT+} of delay stage 32A is shifted 90°, V_{OUT-} of delay stage 32A is shifted 180°, and V_{OUT-} of delay stage 32B is shift[ed] 270°." (*Dai*, Column 3, Lines 54-59).

It is clear that the *Dai* delay stages (32A and 32B) each cause a fixed phase shift of 90°. The value of phase shift is 90° is a fixed value and is not a variable value. Therefore, the delay stages (32A and 32B) of the *Dai* reference are <u>not</u> "variable phase shifting circuits." Because the claims of the Applicants' patent application require a <u>variable</u> phase shifting circuit (and not a fixed phase shifting circuit), the *Dai* reference does not anticipate the Applicants' invention.

The Examiner stated that the transistors M1 and M7 and the cross coupled transistors M5 and M6 in the *Dai* reference form a synchronized oscillator that maintain an oscillation of the

output signal. (August 5, 2008 Office Action, Page 2, Lines 21-23). The Applicants respectfully traverse this assertion of the Examiner. The *Dai* reference states that "The memory element 35 in the configuration shown in FIG. 3 operates to prevent the outputs of inverters 33 and 34 from switching states when they otherwise would switch. In other words, memory element 35 causes switching to be delayed." (*Dai*, Column 5, Lines 58-62). The Applicants respectfully submit that the cross coupled transistors M5 and M6 operate as a memory element 35 and not as a synchronized oscillator.

The cross coupled transistors M5 and M6 constitute a very stable circuit 35 (as it must be for a memory, namely a latch). The electrical state of this memory circuit 35 can only be changed by applying a switching signal at the input. In the absence of such switching signal input to the cross coupled transistors M5 and M6, there will be no variation at the output. Therefore, the memory circuit 35 can not be equivalent to an oscillator circuit.

Furthermore, the *Dai* reference states that "In accordance with the invention, the strength of inverters 33 and 34 is variable and dependent upon the control voltage received by the tuning transistors M1, M4, M7 and M10, whereas the strength of the memory element 35 remains relatively constant as it is tied, in the case of FIG. 3, to the power supply voltage V_{DD}. (*Dai*, Column 5, Line 67 to Column 6, Line 6) (Emphasis added). Because the strength of the memory element 35 remains relatively constant, the memory element 35 is not a synchronized oscillator that has a variable free-running oscillation frequency that is controlled by a control signal. There is no control signal in the *Dai* reference that controls the relatively constant memory element 35. This is because the cross coupled transistors M5 and M6 operate as a memory element 35 and not as a synchronized oscillator.

For these reasons, the elements of the *Dai* reference do not anticipate the Applicants' invention as claimed in Claims 1-2, 24-29 and 33-36. Accordingly, the Applicants respectfully request withdrawal of the §102 anticipation rejections and full allowance of Claims 1-2, 24-29 and 33-36.

As a result of the foregoing, the Applicants respectfully assert that the claims in the Application are in condition for allowance over all art of record, and that the rejections are both factually and legally deficient, and respectfully requests this case be returned to the Examiner for allowance. The Commissioner is hereby authorized to charge any fees connected with this case or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,
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